Mixed Analog-Digital Circuit Modeling Using Event-Driven VHDL

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Abstract

The mixed-signal event-driven (MixED) method developed to simulate small portions of analog circuitry within a digital environment is demonstrated in a mixed signal application. The MixED models using concurrent iteration to account for analog nodes were coded and run in standard VHDL'93. Networks containing linear components such as sources, resistors, capacitors, inductors and operational amplifiers are presented. The possibility to manipulate resistors during runtime is used to simulate switches.

1 Introduction

A new method for mixed-signal event-driven (MixED) circuit modeling was recently presented [1-4]. It allows for behavioral modeling of some analog circuitry containing linear components using an event-driven simulator. The intention is to simulate small analog circuits within a digital environment using an event-driven simulator.

Situations witch need to simulate small portions of analog circuitry within a mostly digital chip are frequently reported, e.g. [5-13]. Examples are the behavior of a pad or specific circuitry, typically located after input pins or before output pins of a chip, e.g. [14-16]. A technique to model high gain operational amplifiers with the presented method is introduced at the same conference [4].

The presented method can be coded in any event-driven HDL that fulfills certain criteria like real number processing, zero-delay simulation deltas and user definable resolution functions. The MixED simulator presented here was coded in standard VHDL'93.

2 Analog Applications with Passive Linear Components

One possible application for the MixED models is the input pad protection system of a typical CMOS input. During normal operation the protection diodes of a CMOS technology can be modeled as an RC filter as shown in Fig. 2.1, that follows the bond wire-pad LC system. According to this model a pad contains two analog nodes. In the example of Fig. 2.2 is L_{wire}=6 nH, C_{pad}=0.28 pF, R_{diff}=60 Ω and C_{diodes}=12 pF. The input capacitance of the buffer is assumed to be $C_{in,buffer} << C_{diodes}$ and can be neglected for this reason.

Figure 2.1:
(a) Possible sketched geometry of input pad and
(b) schematic model.

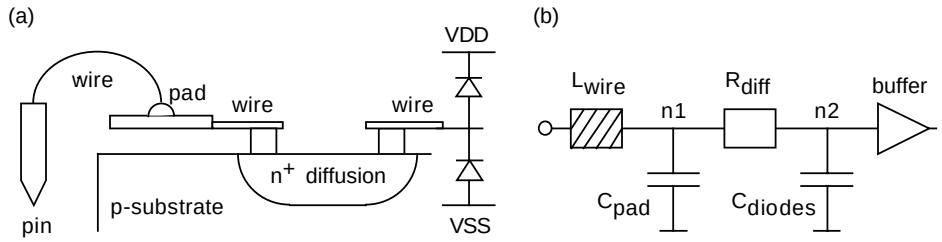


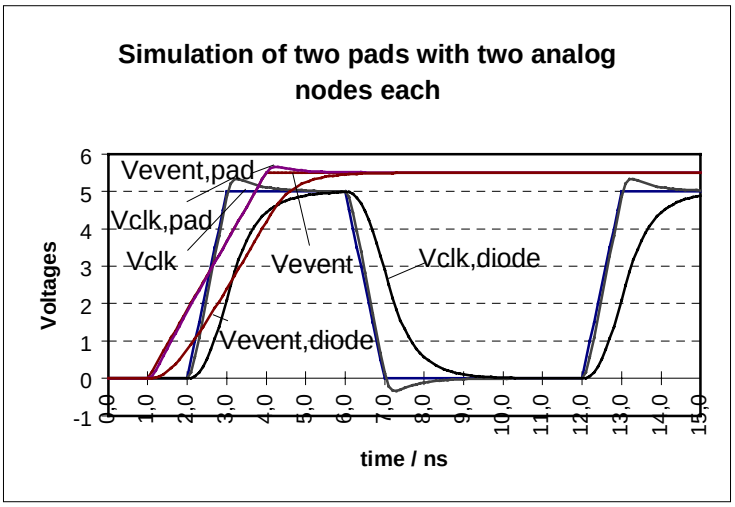
Fig. 2.2 illustrates the distortion of input voltage waveforms due to the pad's RCL circuit. It is known from signal processing theory that very sharp pulses are experienced as Dirac impulses by the filter and cause it to deliver its impulse response. Fig. 2.2 shows the distortion of (1) a 100 MHz clock signal and (2) an asynchronous, rising edge. The two independent events happen at two different input pins but are drawn over each other in Fig. 2.2. This figure explains why the speed of CMOS circuits is typically limited by the input pads. Sometimes phase-locked loops (PLL) are used for synchronous on-chip clock multiplication. In this case the model for the PLL needs some analog circuitry [7].

Figure 2.2:

MixED simulation for two independent pads drawn in one figure:

(1) 100 MHz clock signal distorted by RLC pad system and

(2) asynchronous external event with slow clock edge.



3 Operational Amplifiers in more Complex Mixed-Signal Applications

In this example the MixED models are used for a mixed-signal analog-digital circuit. The digital part is a synchronously clocked state machine. The analog part has to integrate a narrow impulse sensed by a photo diode. To achieve high time resolution due to small junction capacitance the photo diode is reverse biased. So it delivers a narrow current impulse I_{imp}, which is normally translated into a voltage impulse V_{imp}. However, the high capacitance of a CMOS input pad's protection diodes (C_{diodes} in Fig. 3(a)) causes severe distortion of narrow voltage pulses. To avoid voltage steps on C_{diodes}, the voltage integrator of Fig. 3.1(a) was replaced by a current integrator in Fig. 3.1(b). This allows for the removal of resistor R_i (which is not available in a digital standard CMOS technology) on the one hand and avoids the current-to-voltage impulse translation after the photo diode on the other.

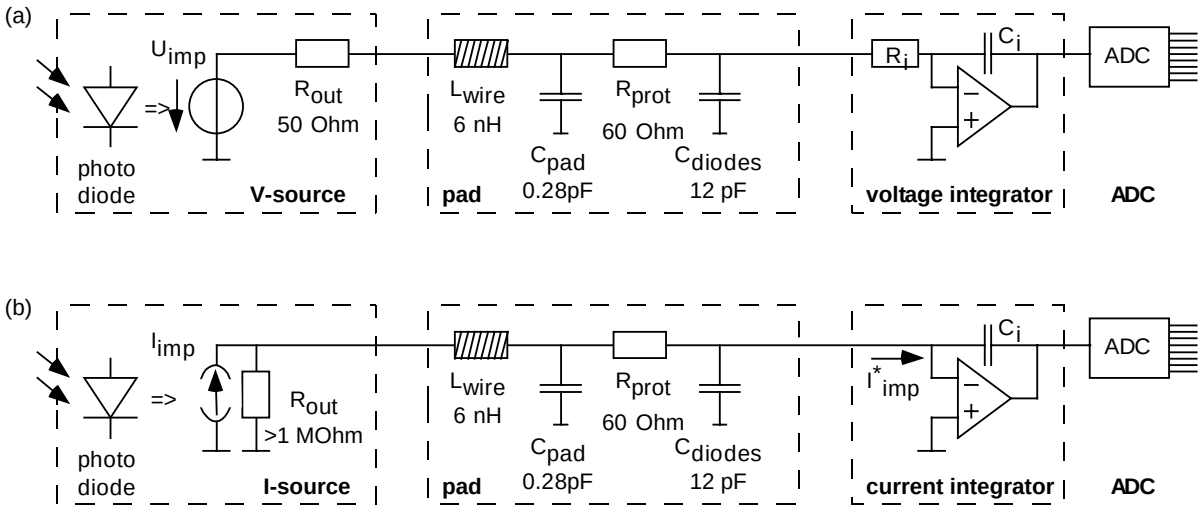


Figure 3.1:
(a) Voltage integration suffering from signal distortion on the pad's RLC system,
(b) Current integration, the voltage over the large capacitor C_{diodes} is kept constant.

Fig. 3.2 gives a more detailed view of the three phases needed to perform the simulation than Fig. 3.1:

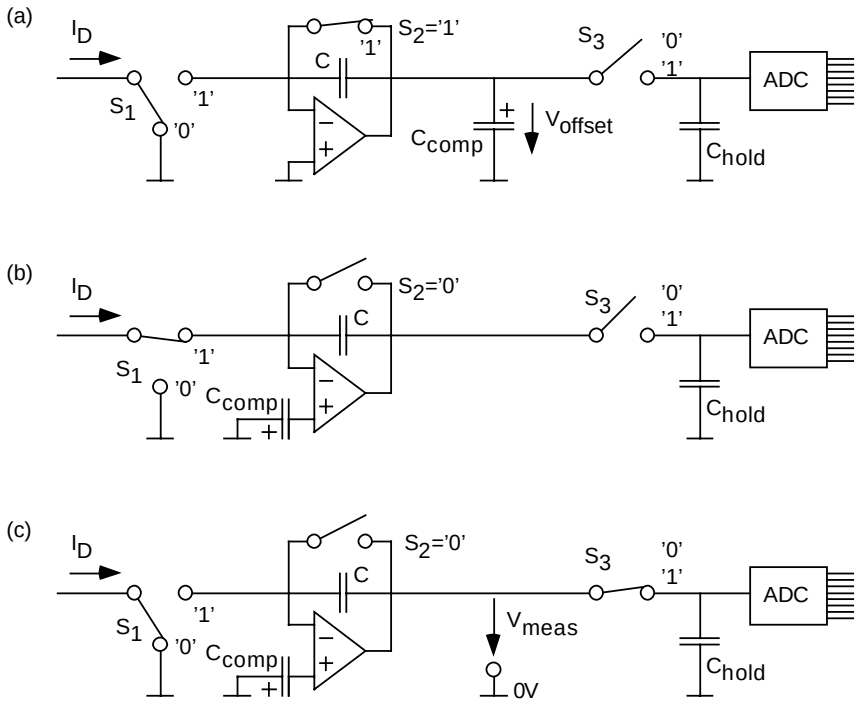
(a) Not-ready for measurement, charging the offset voltage V_{offset} onto the offset compensation capacitor C_{comp}.
(b) Ready to capture the asynchronous current impulse, note that the switch S_3 of the sample and hold ADC is still open.
(c) Measurement ready, the OpAmp's output voltage must be captured into the sample & hold for analog-to-digital conversion, which is triggered when S_3 is opened.

Figure 3.2:

(a) Not-ready mode, charging C_{comp},

(b) ready to capture asynchro-nous event and

(c) taking result over on the sample and hold circuit for A/D conversion.



To realize the switches, advantage is taken of the fact that the MixED models allow for resistor manipulation during runtime. Simulation results are shown in Fig. 3.4.

Figure 3.3:

Digital signals required for the most important switches used in Fig. 3.2.

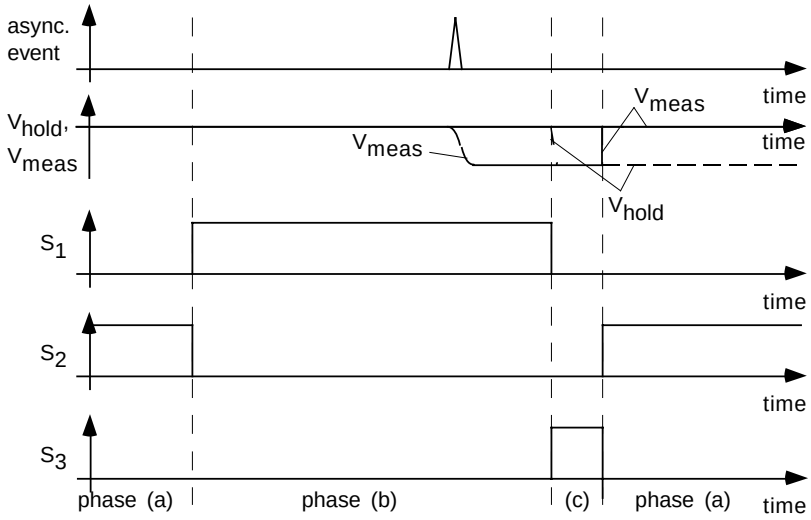
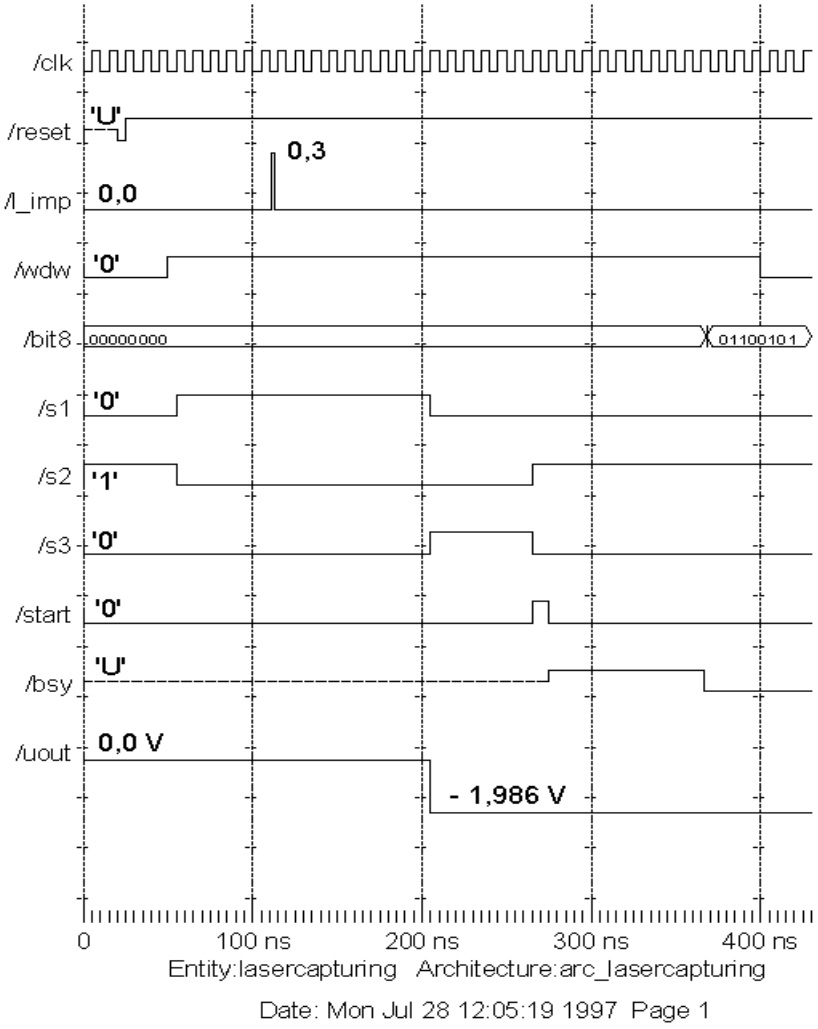


Figure 3.4:

Simulation results obtained using the V-System simulator [17] on a PC



Signal	***Meaning***
clk	clock (f = 100 MHz; T = 10 ns)
reset	global asynchronous reset (for the digital Part: Lc_Controller)
L_imp	photo sensor impulse
wdw	window of valid impulses
bit8	A/D-Converter output (1 byte)
s1	switch control signal #1
s2	switch control signal #2
s3	switch control signal #3
start	start impulse for A/D-conversion
bsy	busy signal of A/D-converter: '1' → not ready, '0' → ready
uout	voltage on C_{hold}

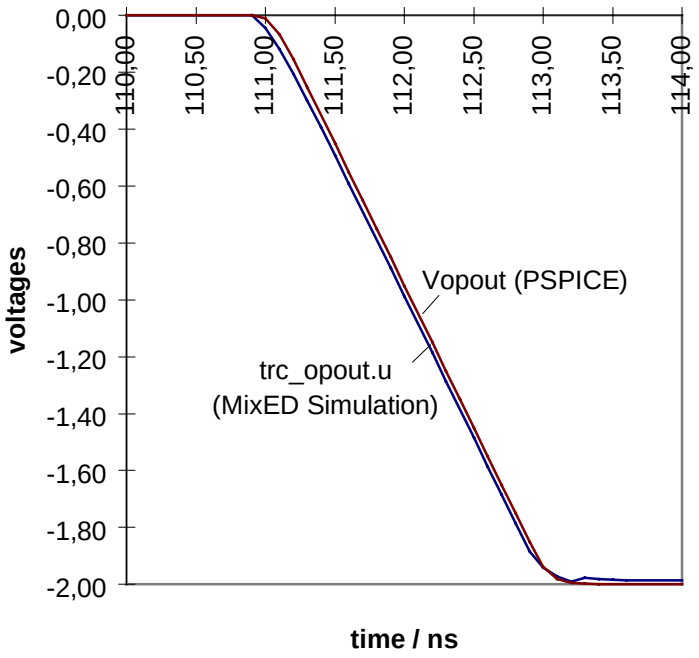
Table 3.1: Signals and their meanings in the figure above.

Graphics were made using a spreadsheet [18] to display ASCII data written by VHDL. Fig. 3.5 compares the results obtained with the MixED simulator to PSpice [19] data taken as reference. The MixED models were compiled and run together with the digital state machine on V-System's VHDL'93. The analog time step was $\Delta t = 0{,}1$ ns.

Figure 3.5:

Detailed view of the falling edge at the integrator's output. The difference between the results of the MixED and the PSpice simulator is small for sufficiently small time steps.

To obtain this figure a constant time step of $\Delta t = 0{,}1$ ns was used.



As shown in Fig. 3.5 the implicit backward Euler integration of the MixED models allows for accurate results if sufficiently small time steps are used. The numerical stability of the employed operational amplifier model according to [4] is excellent. To employ the switches in a numerically effective and stable way needs some experience. In the above simulation infinite switching speed and no need for overlapping clocks was assumed.

Modeling circuits containing MixED models requires some experience and understanding of what is an easy and what a difficult task to solve by the MixED method. More details addressing this matter will be offered soon.

4 Limitations

So far neither adaptive time stepping nor nonlinear MixED devices are available. Work addressing this problems will be presented soon.

Until now the available range of MixED models is limited to passive, linear components (R, L, C), independent sources (U, I) and high-gain operational amplifiers (differential input, single-ended output) to be used in a VHDL environment.

5 Future potential

The MixED components can be coded in any HDL employing an event-driven time axis if certain preconditions are fulfilled (i.e. real number processing, zero delay simulation deltas and user defined resolution functions). Consequently, tools allowing for mixed VHDL & Verilog simulation (e.g.[17]) may be able to offer some unified analog simulation for both HDLs.

Convergence problems in more complex analog circuits may be solved in future, as both MixED models and real devices have no more information about the entire circuit than is available from neighboring components. So a numerically stable solution is not a problem of information availability but only a lack of modeling at this state.

By its nature the presented MixED method allows for dynamic linking and disconnection of components and allows it to be coded for concurrent iteration using several processors.

6 Conclusion

In conclusion, this communication reports the actual range of applications and gives an impression of the practical relevance of event-driven analog circuit modeling. No mixed-signal simulation kernel is necessary. Limitations such as constant time stepping, linearity of models and convergence problems in larger analog circuits are addressed. Future possibilities regarding unified VHDL/Verilog models, adaptive time stepping and non-linear devices as well as the suitability for concurrent iteration on several processors have been discussed.

7 References

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[18] Microsoft Excel 7.0.

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